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TO: Appeal Brief-Patents, USPTO	DATE: February 17, 2006
FROM: Trevor Lind	PAGES INCLUDING COVER: 26
RE: Application Serial No. 09/640,802	FAX NO.: (571)273-8300
OUR FILE NO.: 956.1055	IBM REF. NO.: AUS9-2000-0285-US1

MESSAGE:

RE: SERIAL NO. 09/640,802
GROUP ART UNIT 2634

ATTACHED:
FEE TRANSMITTAL
APPEAL BRIEF

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FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/640,802
Filing Date	August 17, 2000
First Named Inventor	Tai Anh Cao et al.
Examiner Name	Ted M. Wang
Art Unit	2634
Attorney Docket No.	AUS9-2000-0285-US1

METHOD OF PAYMENT (check all that apply)

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1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims _____ - 20 or HP = _____ x _____ = _____ Fee Paid ($)

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims _____ - 3 or HP = _____ x _____ = _____ Fee Paid ($)

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Multiple Dependent Claims: Fee ($) _____ Fee Paid ($) _____

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If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

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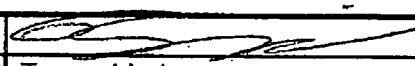
Signature		Registration No. (Attorney/Agent) 54,785	Telephone 512.327.8932
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PATENT
AUS9-2000-0285-US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of: Tai Anh Cao et al.	
Serial No.: 09/640,802	Group Art Unit: 2634
Filed: August 17, 2000	
FOR: CIRCUIT FOR FACILITATING SIMULTANEOUS MULTI-DIRECTIONAL TRANSMISSION OF MULTIPLE SIGNALS BETWEEN MULTIPLE CIRCUITS USING A SINGLE TRANSMISSION LINE	Examiner: Ted M. Wang Facsimile No.: (571) 273-8300

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APPEAL BRIEF

This is an appeal from the Final Office Action mailed September 20, 2005 (the "Final Office Action"), rejecting claims 5, 6, 11, 12, 15, and 16. Appellants submit this Appeal Brief to the Board of Patent Appeals and Interferences within the two-month period following the Notice of Appeal filed December 20, 2005.

This Appeal Brief is accompanied by an authorization (Fee Transmittal form PTO/SB/17) to charge Deposit Account No: 09-0447 for the fee of $500.00 due under 37 C.F.R. §41.20(b)(2), together with any additional fees which may be required for filing this Appeal Brief.

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I. REAL PARTY IN INTEREST (37 C.F.R. §41.37(c)(1)(i))

The above-described patent application is assigned to International Business Machines Corporation ("IBM"), the real party in interest.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. §41.37(c)(1)(ii))

There is no related Appeal or Interference before the United States Patent and Trademark Office.

III. STATUS OF THE CLAIMS (37 C.F.R. §41.37(c)(1)(iii))

The status of the claims is as follows:

Allowed Claims:	1 through 4, 7 through 10, 13, 14, and 18
Claims to which Objections apply:	None
Claims withdrawn from consideration:	None
Claims Rejected:	5, 6, 11, 12, 15, and 16
Claims Appealed:	5, 6, 11, 12, 15, and 16

IV. STATUS OF AMENDMENTS (37 C.F.R. §41.37(c)(1)(iv))

The amendments to the specification filed December 20, 2005, in response to the Examiner's comments and objections in the November 14, 2005 Advisory Action have been entered as indicated by the Advisory Action mailed January 17, 2006.

No amendments to the claims have been filed subsequent to the September 20, 2005 Final Office Action. The claims reproduced in the accompanying Claims Appendix reflect the state of the claims as they currently stand in this case.

V. SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. §41.37(c)(1)(v))

The present invention includes an electronic circuit 104 adapted to send a signal to two or more separate electronic circuits 105 and 106 over a common transmission line 108 while simultaneously receiving signals from the two or more separate electronic circuits 105 and 106 over the common transmission line 108 (p. 7, lines 6-13). The electronic circuit 104 includes signal sending circuitry coupled to an interface node 117 which is adapted to be coupled to the common transmission line 108 (p. 7, lines 24-26; p. 8, lines 5-7). The signal sending circuitry creates a combined signal at the interface node 117 (p. 11, lines 21-23). This combined signal is dependent on the signal from the electronic circuit 104 and the signals simultaneously applied by the two or more separate electronic circuits 105 and 106 connected at other points 118 and 119 to the common transmission line 108 (p. 10, line 24 - p. 11, line 2; p. 8, lines 7-9). The electronic circuit 104 also includes decoding circuitry 110 coupled to the interface node 117 (p. 7, line 26 - p. 8, line 7). This decoding circuitry 110 detects the combined signal at the interface node 117 and decodes the signals from the two or more separate electronic circuits responsive to the combined signal (p. 9 lines 5-20; p. 7, line 26 - p. 8, line 7).

The present invention also includes an electronic circuit arrangement 100 including three or more circuits 104, 105, and 106 connected together by a common transmission line 108, where each circuit 104, 105, and 106 is adapted to assert a respective digital signal (p. 7, lines 6-13).

Each circuit 104, 105, and 106 includes respective sending circuitry connected to the common transmission line 108 and this sending circuitry cooperates to produce an encoded signal on the transmission line 108 based upon the values of the respective digital signals asserted by the respective circuits 104, 105, and 106 (p. 7, line 24 - p. 8, line 9; p. 10, line 24 - p. 11, line 2). The encoded signal comprises one signal from a set of unique encoded signals. Each different signal in the set of encoded signals is representative of a particular combination of digital signals asserted simultaneously from the respective circuits 104, 105, and 106 (p. 11, lines 21-23). Each circuit 104, 105, and 106 also includes a respective decoding arrangement 110, 112, and 114 for decoding the encoded signal appearing on the common transmission line 108 to produce the digital signals asserted from each other circuit 104, 105, and 106 (p. 8, lines 14-23).

Means Plus Function Expressions

Claim 1 elements (a) and (b), claim 7 elements (b) and (c), and claim 13 elements (a) and (b) include means plus function expressions under 35 U.S.C. 112, paragraph six.

Claim 1

Claim 1 element (a) includes the means plus function expression, "...the signal sending circuitry creating a combined signal at the interface node." The structure of the signal sending circuitry of element (a) includes a DRIVER A and encoding element 109 for circuit 104, DRIVER B and encoding element 111 for circuit 105, and DRIVER C and encoding element 113 for circuit 106 (Figures 1-4 and p. 7, line 24 - p. 8, line 5). The encoding elements 109, 111, and

113 are shown as resistors Ra, Rb, Rc, respectively, in Figures 2, 3 and 4 (p. 8, line 26 - p. 9, line 3).

Element (b) of claim 1 includes the means plus function expression, "...the decoding circuitry detecting the combined signal at the interface node and decoding the signals from the two or more separate electronic circuits responsive to the combined signal." Figure 1 shows the decoding circuitry at 110 for circuit 104, at 112 for circuit 105, and at 114 for circuit 106 (p. 7, line 26 - p. 8, line 5). Figure 2 shows a particular decoding circuit 110 made up of a second signal decoding arrangement 201 and a third signal decoding arrangement 204 (p. 9, lines 5-20). Figure 3 shows a particular decoding circuit 112 made up of a first signal decoding arrangement 301 and a third signal decoding arrangement 303 (p. 9, line 21 - p. 10, line 8). Figure 4 shows a particular decoding circuit 114 made up of a first signal decoding arrangement 401 and a second signal decoding arrangement 403 (p. 10, lines 9-23).

Claim 7

Claim 7 element (b) includes the means plus function expression, "...the sending circuitry of the respective circuits cooperating to produce an encoded signal on the transmission line based upon the values of the respective digital signals asserted by the respective circuits." The structure of the sending circuitry of element (b) includes a DRIVER A and encoding element 109 for circuit 104, DRIVER B and encoding element 111 for circuit 105, DRIVER C and encoding element 113 for circuit 106 (Figures 1-4 and p. 7, line 24 - p. 8, line 5). The digital signal encoding elements 109, 111, and 113 are resistors Ra, Rb, Rc, respectively, in Figures 2, 3, and 4 (p. 8, line 26 - p. 9, line 3).

Claim 7 element (c) includes the means plus function expression, "...a decoding arrangement for decoding the encoded signal appearing on the common transmission line to produce the digital signals asserted from each other circuit." Figure 1 shows the decoding circuitry at 110 for circuit 104, at 112 for circuit 105, and at 114 for circuit 106 (p. 7, line 26 - p. 8, line 5). Figure 2 shows a particular decoding circuit 110 made up of a second signal decoding arrangement 201 and a third signal decoding arrangement 204 (p. 9, lines 5-20). Figure 3 shows a particular decoding circuit 112 made up of a first signal decoding arrangement 301 and a third signal decoding arrangement 303 (p. 9, line 21 - p. 10, line 8). Figure 4 shows a particular decoding circuit 114 made up of a first signal decoding arrangement 401 and a second signal decoding arrangement 403 (p. 10, lines 9-23).

Claim 13

Claim 13 element (a) includes the means plus function expression, "...the first, second, and third encoding elements cooperating to produce an encoded signal on the common transmission network based upon the values of the first, second, and third digital signals." The first, second, and third encoding elements 109, 111, and 113 are resistors Ra, Rb, Rc, respectively, in Figures 2, 3, and 4 (p. 8, line 26 - p. 9, line 3).

Element (b) of claim 13 includes the means plus function expression, "...the respective decoding arrangement for each respective circuit for decoding the encoded signal to produce the digital signals produced by each other circuit in the system." Figure 1 shows the decoding circuitry at 110 for circuit 104, at 112 for circuit 105, and at 114 for circuit 106 (p. 7, line 26 - p. 8, line 5). Figure 2 shows a particular decoding circuit 110 made up of a second signal decoding

arrangement 201 and a third signal decoding arrangement 204 (p. 9, lines 5-20). Figure 3 shows a particular decoding circuit 112 made up of a first signal decoding arrangement 301 and a third signal decoding arrangement 303 (p. 9, line 21 - p. 10, line 8). Figure 4 shows a particular decoding circuit 114 made up of a first signal decoding arrangement 401 and a second signal decoding arrangement 403 (p. 10, lines 9-23).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. §41.37(c)(1)(vi))

Claims 5, 6, 11, 12, 15, and 16 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the present invention.

VII. ARGUMENT (37 C.F.R. §41.37(c)(vii))

CLAIMS 5, 6, 11, 12, 15, AND 16 ARE NOT INDEFINITE UNDER 35 U.S.C. §112, SECOND PARAGRAPH

The Final Office Action rejected claims 5, 6, 11, 12, 15, and 16 under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. The Appellants believe this rejection under 35 U.S.C. §112, second paragraph is in error.

All of the Section 112 rejections are made in view of designations in the claims such as "a second differential receiver" where no "first" differential receiver had been previously introduced in the claim or parent claim. *(See* Items 3-8 on pages 3-4 of the Final Office Action.)

The basis for each rejection is summed up in the Final Office Action at page 3, lines 6-10 as follows:

> A second differential receiver without introducing [sic] first differential receiver, and a second and third reference voltage without introducing [sic] first voltage, for example claim 5, make the [sic] claim 5 indefinite [sic] that there is insufficient antecedent basis for the limitation in the claim.

There is No Lack of Antecedent Basis in the Rejected Claims

The Final Office Action appears to reject claims 5, 6, 11, 12, 15, and 16 based on lack of antecedent basis solely in view of the use of a higher ordinal such as "a second element X" where a "first element X" has not been previously referenced in the claim. However, a reference to "a second element X" without any previous reference in the claim to "a first element X" simply does not raise any antecedent basis issue. Rather, indefiniteness from a lack of antecedent basis may arise in some cases when a definite article such as "the" is used to introduce an element for the first time in a claim, or when a definite article is used to reference an element where two or more of the same element have previously been referenced. In these cases it may be unclear as to which particular element is being referenced in the claim. *See* M.P.E.P. §2173.05(e). However, a reference to "a second element X" without any previous reference in the claim to "a first element X" raises no issue regarding clarity as to the structure being claimed, particularly where the claim language matches the language used to define elements in the disclosure, as it does in this case. In addition, each of the currently rejected claims properly introduces each new component with an indefinite article and references each previously introduced component with a definite article. Thus, no antecedent basis issue arises in any of these claims. There is simply never any issue as to which component is being referenced in the claims.

The Meaning and Scope of the Rejected Claims is Clear

The definiteness inquiry under 35 U.S.C. §112, second paragraph, is whether the claim language makes the scope of the claim clear to a hypothetical person possessing the ordinary level of skill in the pertinent art. M.P.E.P. §2171. If the claim language is such that the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite. *Ex parte Porter*, 25 USPQ2d 1144, 1145 (Bd. Pat. App. & Inter. 1992). **Furthermore, the definiteness of language employed in a claim must not be viewed in a vacuum, but always in light of the application disclosure.** *In re Moore and Janoski*, 169 U.S.P.Q. 236, 238 (C.C.P.A. 1971).

In this case, claims 5, 6, 11, 12, 15, and 16 are not indefinite. The meaning and scope of each rejected claim is readily ascertainable simply by reference to the disclosure because the same language used to name components in the claims is also used to reference components in the disclosure. For example, claim 5 refers to "a reference voltage multiplexer connected to receive a first digital signal as a control signal, and having **second and third reference voltage inputs**" and further refers to "**a second differential receiver** having a positive input connected to receive the combined signal, and a negative input connected to receive an output of the reference voltage multiplexer." The second and third reference voltage inputs and the second differential receiver referenced in claim 5 are first identified in the disclosure in the following passage which begins at page 9, line 7 of the disclosure.

> Decoding arrangement 201 includes reference voltage multiplexer 202 and second differential receiver 203. Multiplexer 202 receives second and third reference voltage inputs (V2 and V3) and is controlled by signal A to pass one of those reference voltages to the negative input of second differential receiver 203.

All of the elements in this passage are shown in Figure 2.

Claims 6, 11, 12, 15, and 16 exhibit this same consistency between the terms used in those claims and the terms used in the disclosure for the corresponding circuit components. Therefore, the rejected claims in this case are not indefinite because the direct correspondence between the claim language and the disclosure terminology makes the scope of these claims perfectly clear.

The Manner in which Ordinals Appear in the Claims is a Natural Result of the Nature of the Invention Being Claimed

The electronic circuit which is the subject of the present invention employs multiple instances of certain components such as differential receivers, multiplexers, and reference voltages. The Appellants have chosen to use ordinals (e.g., first, second, third, etc.) to differentiate between similar components. For example, the disclosure refers to a "first differential receiver 302," a "second differential receiver 203," and a "third differential receiver 206." In order to clearly and distinctly claim the subject matter which the Appellants regard as the invention, the Appellants have chosen to maintain the same ordinals in the claims to distinguish between components of the same type.

As shown in Figure 1 of the present application, three circuits are communicating with each other that each have a respective decoding arrangement, 110, 112, or 114. As shown in Figures 2 through 4, each of these decoding arrangements includes a specific decoding circuit for decoding a respective signal from the combined signal. For example, Figure 2 shows a second signal (signal B) decoding circuit 201, while Figure 3 shows a first signal (signal A) decoding circuit 301. The dependent claims in this case are directed to the specific signal decoding circuits

and circuit decoding arrangements shown in Figures 2-4. In some cases, the dependent claims are claiming circuits that do not include a "first" of one element, but do include a "second" or some other higher ordinal of that element. For example, Claim 5 happens to claim the specific second signal (signal B) decoding circuit shown at 201 in Figure 2. A comparison of decoding circuit 201 and the first signal (signal A) decoding circuit 301 (Figure 3) reveals that circuit 201 does not include the element referenced as the first reference voltage V1. Thus, since claim 5 is directed to decoding circuit 201, claim 5 does not describe a first reference voltage input, but does refer to the second and third reference voltage inputs. Also, although decoding circuit 201 includes the second differential receiver 203, it does not require the component disclosed as the first differential receiver, which is shown at 302 in Figure 3 and described in the disclosure at page 9, lines 15-17. Thus, claim 5 refers to "a second differential receiver" but does not refer to the first differential receiver.

Similarly to claim 5, claims 6, 11, 12, 15, and 16 are each directed to circuits that include elements designated with higher ordinals in the disclosure (e.g. "a third differential receiver") but do not include the elements designated with the corresponding lower ordinals (e.g. "a first differential receiver" or "a second differential receiver"). As is the case with claim 5, the use of ordinals in this manner is a natural result of the components of the respective decoding circuits required by these claims in light of the overall structure of the present invention.

The use of ordinals in the claims as described above does not make the claims indefinite under 35 U.S.C. §112, second paragraph because the meaning of claims 5, 6, 11, 12, 15, and 16 is not ambiguous and the language used in these claims clearly and precisely claims the subject matter that the Appellants regard as the invention. The meaning and scope of each rejected claim

is readily ascertainable simply by reference to the disclosure because the same language used to name components in the claims is also used to reference components in the disclosure. Thus, for example, it is clear that the "second differential receiver" referenced in claim 5 refers to the second differential receiver of the signal B decoding circuitry shown in Figures 2 and 4. Therefore, since the scope of claims 5, 6, 11, 12, 15, and 16 is abundantly clear when considered in view of the application disclosure and since there are no antecedent basis issues relating to the rejected claims, these claims are by no means indefinite under 35 U.S.C. §112, second paragraph.

VIII. CONCLUSION

For all of the above reasons, the Appellants submit that claims 5, 6, 11, 12, 15, and 16 are entitled to allowance, and respectfully request that the Board reverse the decision of the Examiner rejecting these claims.

Respectfully submitted,

The Culbertson Group, P.C.

Date: 2/17/06

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IX. CLAIMS APPENDIX (37 C.F.R. §41.37(c)(1)(viii))

1. An electronic circuit adapted to send a signal to two or more separate electronic circuits over a common transmission line while simultaneously receiving signals from the two or more separate electronic circuits over the common transmission line, the electronic circuit comprising:

(a) signal sending circuitry coupled to an interface node which is adapted to be coupled to the common transmission line, the signal sending circuitry creating a combined signal at the interface node, the combined signal being dependent on the signal from the electronic circuit and the signals simultaneously applied by the two or more separate electronic circuits connected at other points to the common transmission line; and

(b) decoding circuitry coupled to the interface node, the decoding circuitry detecting the combined signal at the interface node and decoding the signals from the two or more separate electronic circuits responsive to the combined signal.

2. The electronic circuit of Claim 1 wherein the signal sending circuitry comprises:

(a) a signal driver; and

(b) an encoding element connected between the signal driver and the interface node.

3. The electronic circuit of Claim 2 wherein the encoding element comprises a resistor.

4. The electronic circuit of Claim 1 wherein the decoding circuitry comprises:

(a) a first differential receiver having a positive input connected to receive the combined signal and having a negative input connected to a first reference voltage source.

5. The electronic circuit of Claim 1 wherein the decoding circuitry comprises:

(a) a reference voltage multiplexer connected to receive a first digital signal as a control signal, and having second and third reference voltage inputs;

(b) a second differential receiver having a positive input connected to receive the combined signal, and a negative input connected to receive an output of the reference voltage multiplexer.

6. The electronic circuit of Claim 1 wherein the decoding circuitry comprises:

(a) an additional reference voltage multiplexer connected to be controlled by a first digital signal and a second digital signal and having fourth, fifth, sixth, and seventh reference voltage inputs; and

(b) a third differential receiver having a positive input connected to receive the combined signal and a negative input connected to receive an output from the additional reference voltage multiplexer.

7. An electronic circuit arrangement comprising:

(a) three or more circuits connected together by a common transmission line, each circuit adapted to assert a respective digital signal;

(b) each circuit including sending circuitry connected to the common transmission line, the sending circuitry of the respective circuits cooperating to produce an encoded signal on the transmission line based upon the values of the respective digital signals asserted by the respective circuits, the encoded signal comprising one signal from a set of unique encoded signals with each different signal in the set being representative of a particular combination of digital signals asserted simultaneously from the respective circuits; and

(c) each circuit further including a decoding arrangement for decoding the encoded signal appearing on the common transmission line to produce the digital signals asserted from each other circuit.

8. The electronic circuit arrangement of Claim 7 wherein each circuit is located on a separate integrated circuit chip and the common transmission line comprises a conductor connected to a single electrode on each separate integrated circuit chip.

9. The electronic circuit arrangement of Claim 7 wherein the signal sending circuitry in each respective circuit includes an encoding element comprising a resistor.

10. The electronic circuit arrangement of Claim 7 wherein the three or more circuits includes a first circuit providing a first digital signal, a second circuit providing a second digital signal, and a third circuit providing a third digital signal, and wherein the decoding arrangement associated with the second and third circuits includes a first digital signal decoding arrangement comprising:

(a) a first differential receiver having a positive input connected to receive the encoded signal and having a negative input connected to a first reference voltage source.

11. The electronic circuit arrangement of Claim 7 wherein the three or more circuits includes a first circuit providing a first digital signal, a second circuit providing a second digital signal, and a third circuit providing a third digital signal, and wherein the decoding arrangement associated with the first and third circuits includes a second digital signal decoding arrangement comprising:

(a) a reference voltage multiplexer connected to receive the first digital signal as a control signal, and having second and third reference voltage inputs;

(b) a second differential receiver having a positive input connected to receive the encoded signal, and a negative input connected to receive an output of the reference voltage multiplexer.

12. The electronic circuit arrangement of Claim 7 wherein the three or more circuits includes a first circuit providing a first digital signal, a second circuit providing a second digital

signal, and a third circuit providing a third digital signal, and wherein the decoding arrangement associated with the first and second circuits includes a third digital signal decoding arrangement comprising:

(a) an additional reference multiplexer connected to be controlled by the first digital signal and second digital signal, and having fourth, fifth, sixth, and seventh reference voltage inputs; and

(b) a third differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive an output from the additional reference voltage multiplexer.

13. An electronic system having a first circuit producing a first digital signal, a second circuit producing a second digital signal, and a third circuit producing a third digital signal, the system comprising:

(a) a first circuit encoding element included in the first circuit, a second circuit encoding element included in the second circuit, and a third circuit encoding element included in the third circuit, each respective encoding element connected between a digital signal output of the respective circuit and a common transmission network between the first, second, and third circuits, the first, second, and third encoding elements cooperating to produce an encoded signal on the common transmission network based upon the values of the first, second, and third digital signals, the encoded signal comprising one signal from a set of unique

encoded signals with each different signal in the set being representative of a particular combination of the first, second, and third digital signals; and

(b) a first circuit decoding arrangement included with the first circuit, a second circuit decoding arrangement included with the second circuit, and a third circuit decoding arrangement included with the third circuit, the respective decoding arrangement for each respective circuit for decoding the encoded signal to produce the digital signals produced by each other circuit in the system.

14. The electronic system of Claim 13 wherein the encoding elements each comprise a resistor.

15. The electronic system of Claim 13 wherein the first circuit decoding arrangement comprises:

(a) a reference voltage multiplexer connected to be controlled by the first digital signal and connected to receive second and third reference voltage signals as inputs;

(b) a second differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive a reference voltage multiplexer output;

(c) an additional reference voltage multiplexer connected to be controlled by the first digital signal and the second digital signal, and connected to receive fourth, fifth, sixth, and seventh reference voltage signals as inputs; and

(d) a third differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive an output of the additional reference voltage multiplexer.

16. The electronic system of Claim 13 wherein the second circuit decoding arrangement comprises:

(a) a first differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive a first reference voltage signal;

(b) an additional reference voltage multiplexer connected to be controlled by the first digital signal and the second digital signal, and connected to receive fourth, fifth, sixth, and seventh reference voltage signals as inputs; and

(c) a third differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive an output of the additional reference voltage multiplexer.

18. The electronic system of Claim 13 wherein the third circuit decoding arrangement comprises:

(a) a first differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive a first reference voltage signal;

(b) a reference voltage multiplexer connected to be controlled by the first digital signal and connected to receive second and third reference voltage signals as inputs; and

(c) a second differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive an output of the reference voltage multiplexer.

X. EVIDENCE APPENDIX (37 C.F.R. §41.37(c)(1)(ix))

The Appellants have not relied upon any evidence in this appeal according to 37 C.F.R. §41.37(c)(1)(ix) in order to overcome the currently outstanding grounds of rejection in the case.

XI. RELATED PROCEEDINGS APPENDIX (37 C.F.R. §41.37(c)(1)(x))

There is no related Appeal or Interference before the United States Patent and Trademark Office.